REMARKS

Claims 1-20 are pending in the above-captioned patent application. Claims 1, 10, 16 and 19 are independent claims.

Applicant amended independent claim 1 to clarify that branching to an instruction at a specified address is performed if a state, indicating the availability of a resource of the data processing apparatus, is a specified value. Support for this clarification is found, for example, on page 14, lines 14-17, page 5, etc. The applicant similarly amended independent claims 10, 16, and 19. Applicant also cancelled claim 6 without prejudice.

The examiner rejected claims 1 and 19 under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential elements. The examiner further rejected claims 1 and 19 under 35 U.S.C. §101 on the ground that the invention is allegedly directed to non-statutory subject matter in that the claims are not limited to tangible embodiments.

The applicant thus additionally amended claim 1 to remove the wording "tangibly embodied in an information carrier," and further amended claims 1 and 19 to clarify that the computer program product resides on a computer readable medium that comprises instructions. Amended claims 1 and 19 therefore specify the nature of the information carrier and/or medium (namely, a computer readable medium on which computer instructions can be stored) corresponding to the computer program product. Additionally, the amended claims are limited only to tangible embodiments, namely, a computer program product residing on a computer-readable medium. The applicant thus traverses the examiner's rejection of claims 1 and 19 under 35 U.S.C. §101 and §112, second paragraph.

The applicant further notes that the language in the preamble of amended claims 1 and 19 conforms to the conventional form widely used to recite computer program product claims. Such claims are regularly used and appear in numerous issued patents including, for example, recently issued U.S. Patent Nos. 6,961,787, 6,961,686, and 6,954,833.

The examiner rejected claims 1, 10 and 19 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,275,508 to Aggarwal. The examiner also rejected claims 1-20 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,724,563 to Hasegawa, and further rejected claim 1 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,640,538 to Dyer.

Applicant's independent claim 1 recites the feature of "cause an executing instruction stream to branch to an instruction at a specified address if a state, of a specified state name, the state indicating the availability of a resource of the data processing apparatus, is a specified value." Thus, a decision to branch to a specified address depends on the availability of a resource, identified by a state name, of the data processing apparatus. For example, in some embodiments a decision to branch depends on whether the RCV_REQ FIFO queue has available room to receive another request (page 14, line 15-17 of the originally filed application). Thus, in such embodiments, branching to another address would depend on the state of the rec_req_avail state name, which indicates whether room on the RCV_REQ FIFO queue is available.

In contrast, none of the references cited by the examiner discloses or suggests a branching operation that depends on the availability of a resource of the data processing apparatus.

Aggarwal describes a system for processing datagram headers during traverses from one interface of a networking device to another (Abstract). Aggarwal system includes a sequencer unit that controls the selection of data from input data stream (FIGS. 1 and 12, and Abstract). The sequencer unit is controlled by a word instruction called the Write Control Store (WCS) (see col. 3, lines 61-63). As described in Aggarwal, the WCS includes various fields, shown in FIG. 12, amongst which is a conditional branch field. Aggarwal explains that the condition branch tells the sequencer unit "to jump to one of the multiple addresses in its address field, each one representing the next possible address, if the current instruction is a Conditional Branch ..." (col. 10, lines 24-27). No additional explanations regarding Aggarwal's conditional branch are provided.

Thus, although Aggarwal mentions a branch instruction, at no point does Aggarwal indicate under what circumstances, or on what basis that conditional branch instruction is performed. Therefore, Aggarwal does not disclose branching to an address stream if a state of a specified state name is a specified value. Additionally, Aggarwal does not disclose or suggest branching to another address if a state indicating the availability of a resource of the data processing apparatus is a specified value, as required by applicant's independent claim 1.

Hasegawa discloses a pipeline processor that can execute predictive branch instructions (Abstract). As shown in FIG. 9, and as described in column 11, predictive branching is

performed based on the execution result 109 produced by executing an instruction on execution section 11 of Hasegawa's pipeline processor. Specifically, the execution of an instruction on execution section 11 causes a number of flags to be set in accordance with the result outcome produced by the execution of the instruction (col. 11, lines 25-32). These flags include the Zero flag Z, the negative flag N, the Carryover flag C, and the overflow flag V. For example, if the execution of an instruction produces a negative value, the N flag would be set. Thus, Hasegawa's branching operation is based on the values of result flags generated after a particular instruction was executed. Nowhere does Hasegawa describe that a branching operation depends on the availability of a resource of the data processing apparatus. So Hasegawa does not disclose or suggest branching "to an instruction at a specified address if a state of a specified state name, the state indicating the availability of a resource of the data processing apparatus, is a specified value", as required by applicant's independent claim 1.

Dyer describes a programmable timing mark sequencer that automatically analyzes a sequence of data bits on a data input line (Abstract). Dyer's programmable timing mark sequencer uses an instruction whose format is described in FIG. 8. As shown in Table 1, describing the fields of the instruction shown in FIG. 8, the instruction includes a Branch Address field which specifies the branch address that is taken if the branch condition specified in the Branch Type field is true (col. 11, lines 6-8). As Dyer further describes, if the Branch Type field is set to 1, the branching operation is unconditional, whereas if the Branch Type field is set to 0 then branching will be performed on the presence of bit HRBIT (which is the high resolution bit input line used to drive the timing mark sequencer). With respect to the HRBIT signal, Dyer explains, "[i]f the appropriate timing pattern is detected in the sequence of high resolution data bits HRBIT, timing mark sequencer 240 drives servo timing mark signal STM active" (col. 6, lines 45-48). Thus, the conditional branch operation described in Dyer is based only on the presence of a time-dependent HRBIT signal associated with incoming input data. Dyer, therefore, does not disclose or suggest that the branching operation depends on the availability of a resource of the system. Thus, Dyer does not disclose or suggest the feature of "branch to an instruction at a specified address if a state, of a specified state name, the state indicating the availability of a resource of the data processing apparatus, is a specified value", as required by applicant's independent claim 1.

Since none of the references cited by the Examiner discloses or suggests, alone or in combination, at least the feature of "cause an executing instruction stream to branch to an instruction at a specified address if a state, of a specified state name, the state indicating the availability of a resource of the data processing apparatus, is a specified value", independent claim 1 is therefore patentable over the cited prior art. Claims 2-9 depend from independent claim 1 and are therefore patentable for at least the same reasons as independent claim 1.

Independent claims 10, 16 and 19 recite the feature of "evaluating a value of a specified state name, the value of the state name indicating the availability of a resource of the processor," or similar language. At least this feature is not disclosed by the prior art cited by the examiner for reasons similar to those provided with respect to independent claim 1. Accordingly, Independent claims 10, 16, and 19 are patentable over the prior art.

Claims 11-15 depend from independent claim 10 and are therefore patentable for at least the same reasons as independent claim 10. Claims 17-18 depend from independent claim 16 and are therefore patentable for at least the same reasons as independent claim 16. Claim 20 depends from independent claim 19 and is therefore patentable for at least the same reasons as independent claim 19.

Additionally, the examiner rejected claim 9 under U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,724,563 to Hasegawa. Specifically, the examiner argued that:

> **As to claims 8, 9 Hasegawa alos [sic] included performing the branch based on specified name (see branch on over flow set and branch on overflow clear in Table 1, see the flags set and reset in col.l 1 [sic] lines 14-35, see also the encoded flags in col.1, lines 42-52). As to the parallel processor, see the pipeline processor in col. 5, lines 30-31. [Paragraph 14, page 5 of the August 16, 2005, Office Action]**

Claim 9, which depends from independent claim 1, recites the feature "wherein the state name is the name assigned to an executing context." Thus, branching to a specified address takes place, for example, based on whether or not a specified context is executing (thereby basing the branching decision on the availability of the data processor apparatus' processing capabilities, or resources).

As noted above, Hasegawa conditional branches are based on the values of a number of flags that reflect the outcome that resulted from the execution of an instruction. Hasegawa, therefore, does not base its branching decisions on the state of a specified state name indicating

the availability of a resource of the data processing apparatus, and certainly does not base branching decision on whether or not a particular named context is executing, as required by applicant's claim 9. Accordingly, claim 9 is patentable over the cited art.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

No fee is believed due. Please apply any charges or credits to deposit account 06-1050, referencing attorney docket 10559-306US1.

Respectfully submitted,

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